

1 CLAIM LISTING

2
3 1. (Currently Amended) An first electronic circuit adapted to communicate a signal to a
4 plurality of two or more additional electronic circuits over a common transmission line
5 while simultaneously receiving additional signals from the plurality of two or more
6 additional electronic circuits over the common transmission line, the first electronic
7 circuit including:

8 (a) signal sending circuitry coupled to an interface node which is adapted to be
9 coupled to the common transmission line, the signal sending circuitry for applying
10 a signal from the first electronic circuit to cooperate in creating a combined signal
11 at the interface node, the combined signal being dependent upon the signal from
12 the first electronic circuit and the additional signals simultaneously applied by the
13 plurality of two or more additional electronic circuits connected at other points on
14 the common transmission line; and

15 (b) decoding circuitry coupled to the interface node, the decoding circuitry for
16 detecting the combined signal at the interface node and decoding the additional
17 signals from the combined signal, the additional signals being simultaneously
18 applied by the two or more additional electronic circuits separate from the first
19 electronic circuit.
20

21 2. (Currently Amended) The first electronic circuit of Claim 1 wherein the signal sending
22 circuitry includes:

- 1 (a) a signal driver; and
- 2 (b) an encoding element connected between the signal driver and the interface node.
- 3
- 4 3. (Currently Amended) The first electronic circuit of Claim 2 wherein the encoding element
- 5 comprises a resistor.
- 6
- 7 4. (Currently Amended) The first electronic circuit of Claim 1 wherein the decoding
- 8 circuitry includes:
- 9 (a) a first differential receiver having a positive input connected to receive the
- 10 combined signal and having a $a[[n]]$ negative input connected to a first reference
- 11 voltage source.
- 12
- 13 5. (Currently Amended) The first electronic circuit of Claim 1 wherein the decoding
- 14 circuitry includes:
- 15 (a) a reference voltage multiplexer connected to receive a first digital signal as a
- 16 control signal, and having second and third reference voltage inputs;
- 17 (b) a second differential receiver having a positive input connected to receive the
- 18 combined signal, and a negative input connected to receive an output of the
- 19 reference voltage multiplexer.
- 20
- 21 6. (Currently Amended) The first electronic circuit of Claim 1 wherein the decoding
- 22 circuitry includes:

- 1 (a) an additional reference multiplexer connected to be controlled by a first digital
2 signal and a second digital signal and having fourth, fifth, sixth, and seventh
3 reference voltage inputs; and
4 (b) a third differential receiver having a positive input connected to receive the
5 combined signal and a[[n]] negative input connected to receive an output from the
6 additional reference voltage multiplexer.
7

8 7. (Currently Amended) An electronic circuit arrangement including:

- 9 (a) [[a]] three or more circuits connected together by a common transmission line,
10 each circuit adapted to assert a respective digital signal;
11 (b) each circuit including sending circuitry connected to the common transmission
12 line, the sending circuitry of the respective circuits cooperating to produce an
13 encoded signal on the transmission line based upon the values of the respective
14 digital signals asserted by the respective circuits, the encoded signal comprising
15 one signal from a set of unique encoded signals with each different signal in the
16 set being representative of a particular combination of digital signals asserted
17 simultaneously from the respective circuits; and
18 (c) each circuit further including a decoding arrangement for decoding the encoded
19 signal appearing on the common transmission line to produce the digital signals
20 asserted from each other circuit.
21

1 8. (Original) The electronic circuit arrangement of Claim 7 wherein each circuit is located
2 on a separate integrated circuit chip and the common transmission line comprises a
3 conductor connected to a single electrode on each separate integrated circuit chip.
4

5 9. (Original) The electronic circuit arrangement of Claim 7 wherein the signal sending
6 circuitry in each respective circuit includes an encoding element comprising a resistor.
7

8 10. (Currently Amended) The electronic circuit arrangement of Claim 7 wherein the plurality
9 of three or more circuits includes a first circuit providing a first digital signal, a second
10 circuit providing a second digital signal, and a third circuit providing a third digital
11 signal, and wherein the decoding arrangement associated with the second and third
12 circuits includes a first digital signal decoding arrangement comprising:
13 (a) a first differential receiver having a positive input connected to receive the
14 encoded signal and having a $[[n]]$ negative input connected to a first reference
15 voltage source.
16

17 11. (Currently Amended) The electronic circuit arrangement of Claim 7 wherein the plurality
18 of three or more circuits includes a first circuit providing a first digital signal, a second
19 circuit providing a second digital signal, and a third circuit providing a third digital
20 signal, and wherein the decoding arrangement associated with the first and third circuits
21 includes a second digital signal decoding arrangement comprising:

- 1 (a) a reference voltage multiplexer connected to receive the first digital signal as a
2 control signal, and having second and third reference voltage inputs;
3 (b) a second differential receiver having a positive input connected to receive the
4 encoded signal, and a[[n]] negative input connected to receive an output of the
5 reference voltage multiplexer.
6

7 12. (Currently Amended) The electronic circuit arrangement of Claim 7 wherein the plurality
8 of three or more circuits includes a first circuit providing a first digital signal, a second
9 circuit providing a second digital signal, and a third circuit providing a third digital
10 signal, and wherein the decoding arrangement associated with the first and second circuits
11 includes a third digital signal decoding arrangement comprising:

- 12 (a) an additional reference multiplexer connected to be controlled by the first digital
13 signal and second digital signal, and having fourth, fifth, sixth, and seventh
14 reference voltage inputs; and
15 (b) a third differential receiver having a positive input connected to receive the
16 encoded signal and a[[n]] negative input connected to receive an output from the
17 additional reference voltage multiplexer.
18

19 13. (Original) An electronic system having a first circuit producing a first digital signal, a
20 second circuit producing a second digital signal, and a third circuit producing a third
21 digital signal, the system including:

- 1 (a) a first circuit encoding element included in the first circuit, a second circuit
2 encoding element included in the second circuit, and a third circuit encoding
3 element included in the third circuit, each respective encoding element connected
4 between a digital signal output of the respective circuit and a common
5 transmission network between the first, second, and third circuits, the first,
6 second, and third encoding elements cooperating to produce an encoded signal on
7 the common transmission network based upon the values of the first, second, and
8 third digital signals, the encoded signal comprising one signal from a set of unique
9 encoded signals with each different signal in the set being representative of a
10 particular combination of the first, second, and third digital signals; and
11 (b) a first circuit decoding arrangement included with the first circuit, a second circuit
12 decoding arrangement included with the second circuit, and a third circuit
13 decoding arrangement included with the third circuit, the decoding arrangement
14 for each respective circuit for decoding the encoded signal to produce the digital
15 signals produced by each other circuit in the system.
16

17 14. (Original) The electronic system of Claim 13 wherein the encoding elements each
18 comprise a resistor.
19

20 15. (Original) The electronic system of Claim 13 wherein the first circuit decoding
21 arrangement includes:

- 1 (a) a reference voltage multiplexer connected to be controlled by the first digital
2 signal and connected to receive second and third reference voltage signals as
3 inputs;
- 4 (b) a second differential receiver having a positive input connected to receive the
5 encoded signal and a negative input connected to receive a reference voltage
6 multiplexer output;
- 7 (c) an additional reference voltage multiplexer connected to be controlled by the first
8 digital signal and the second digital signal, and connected to receive fourth, fifth,
9 sixth, and seventh reference voltage signals as inputs; and
- 10 (d) a third differential receiver having a positive input connected to receive the
11 encoded signal and a negative input connected to receive an output of the
12 additional reference voltage multiplexer.

13
14 16. (Original) The electronic system of Claim 13 wherein the second circuit decoding
15 arrangement includes:

- 16 (a) a first differential receiver having a positive input connected to receive the
17 encoded signal and a negative input connected to receive a first reference voltage
18 signal;
- 19 (b) an additional reference voltage multiplexer connected to be controlled by the first
20 digital signal and the second digital signal, and connected to receive fourth, fifth,
21 sixth, and seventh reference voltage signals as inputs; and

1 (c) a third differential receiver having a positive input connected to receive the
2 encoded signal and a negative input connected to receive an output of the
3 additional reference voltage multiplexer.
4

5 17. (canceled)
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7 18. (New) The electronic system of Claim 13 wherein the third circuit decoding arrangement
8 includes:

9 (a) a first differential receiver having a positive input connected to receive the
10 encoded signal and a negative input connected to receive a first reference voltage
11 signal;

12 (b) a reference voltage multiplexer connected to be controlled by the first digital
13 signal and connected to receive second and third reference voltage signals as
14 inputs; and

15 (c) a second differential receiver having a positive input connected to receive the
16 encoded signal and a negative input connected to receive an output of the
17 reference voltage multiplexer.
18

19 19. (New) An electronic circuit arrangement including:

20 (a) a first circuit, a second circuit, and a third circuit connected together by a common
21 transmission line, the first circuit being adapted to assert a first digital signal, the

1 second circuit being adapted to assert a second digital signal, and the third circuit
2 being adapted to assert a third digital signal;

3 (b) the first circuit, second circuit, and third circuit each including sending circuitry
4 connected to the common transmission line, the sending circuitry of the respective
5 first, second, and third circuits cooperating to produce an encoded signal on the
6 transmission line based upon the value of the first digital signal, second digital
7 signal, and third digital signal, the encoded signal comprising one signal from a
8 set of unique encoded signals with each different signal in the set being
9 representative of a particular combination of digital signals asserted
10 simultaneously from the first circuit, second circuit, and third circuit; and

11 (c) the first circuit, second circuit, and third circuit each further including a decoding
12 arrangement for decoding the encoded signal appearing on the common
13 transmission line to produce the digital signals asserted from each other circuit,
14 and

15 (d) wherein the decoding arrangement associated with the first and second circuits
16 includes a third digital signal decoding arrangement comprising an additional
17 reference multiplexer connected to be controlled by the first digital signal and
18 second digital signal, and having fourth, fifth, sixth, and seventh reference voltage
19 inputs, and a third differential receiver having a positive input connected to
20 receive the encoded signal and a negative input connected to receive an output
21 from the additional reference voltage multiplexer.
22

1 20. (New) An electronic system having a first circuit producing a first digital signal, a second
2 circuit producing a second digital signal, and a third circuit producing a third digital
3 signal, the system including:

4 (a) a first circuit encoding element included in the first circuit, a second circuit
5 encoding element included in the second circuit, and a third circuit encoding
6 element included in the third circuit, each respective encoding element connected
7 between a digital signal output of the respective circuit and a common
8 transmission network between the first, second, and third circuits, the first,
9 second, and third encoding elements cooperating to produce an encoded signal on
10 the common transmission network based upon the values of the first, second, and
11 third digital signals, the encoded signal comprising one signal from a set of unique
12 encoded signals with each different signal in the set being representative of a
13 particular combination of the first, second, and third digital signals; and

14 (b) a first circuit decoding arrangement included with the first circuit, a second circuit
15 decoding arrangement included with the second circuit, and a third circuit
16 decoding arrangement included with the third circuit, the decoding arrangement
17 for each respective circuit for decoding the encoded signal to produce the digital
18 signals produced by each other circuit in the system, and

19 (c) wherein the second circuit decoding arrangement includes a first differential
20 receiver having a positive input connected to receive the encoded signal and a
21 negative input connected to receive a first reference voltage signal, an additional
22 reference voltage multiplexer connected to be controlled by the first digital signal

1 and the second digital signal, and connected to receive fourth, fifth, sixth, and
2 seventh reference voltage signals as inputs, and a third differential receiver having
3 a positive input connected to receive the encoded signal and a negative input
4 connected to receive an output of the additional reference voltage multiplexer.